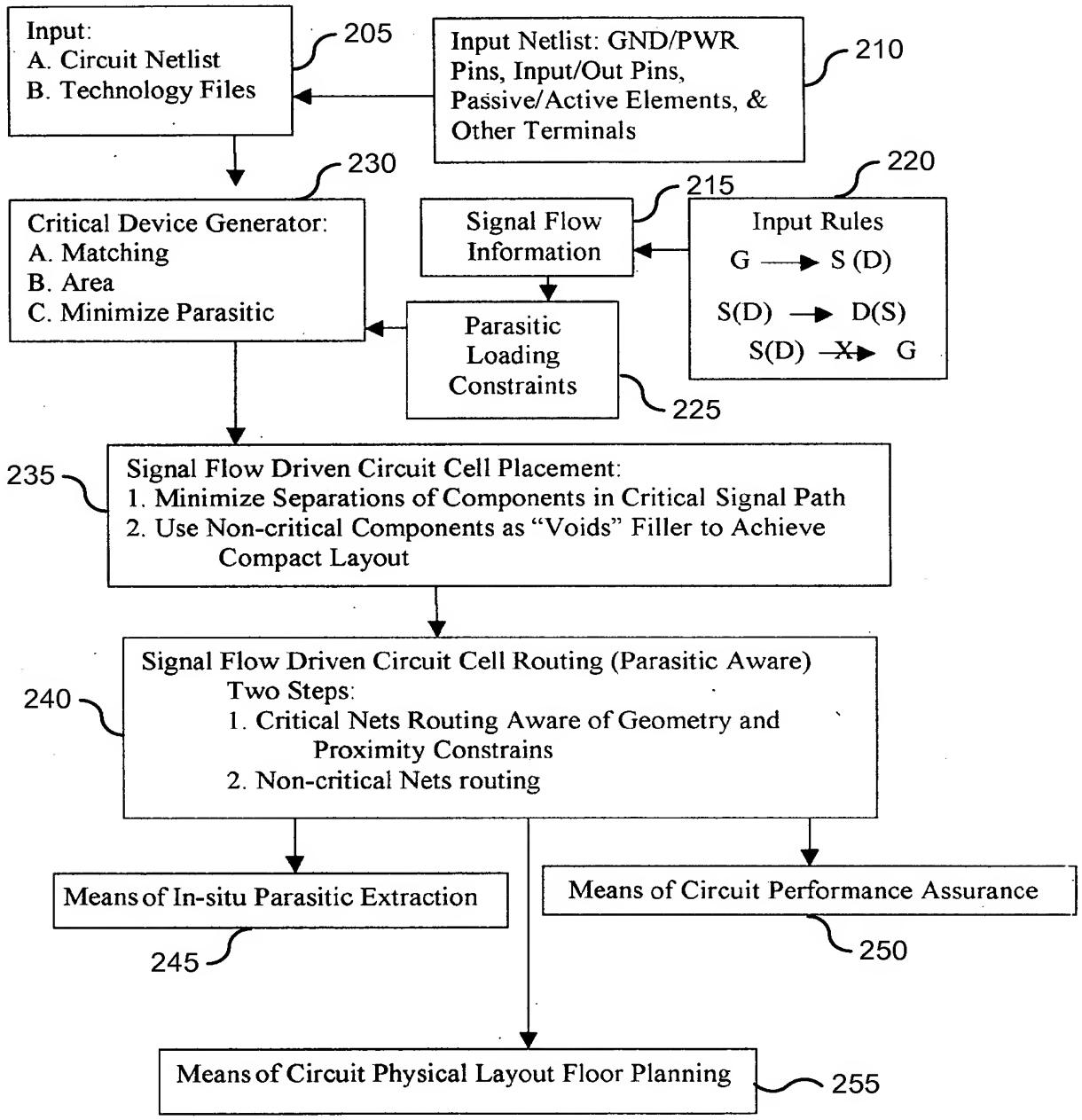
Input:
A. Circuit Netlist
B. Technology Files
205
Input Netlist: GND/PWR Pins, Input/Out Pins, Passive/Active Elements, & Other Terminals
210
230
Critical Device Generator:
A. Matching
B. Area
C. Minimize Parasitic
215
Signal Flow Information
220
Input Rules
G → S (D)
S(D) → D(S)
S(D) → X G
Parasitic Loading Constraints
225
235
Signal Flow Driven Circuit Cell Placement:
1. Minimize Separations of Components in Critical Signal Path
2. Use Non-critical Components as "Voids" Filler to Achieve Compact Layout
240
Signal Flow Driven Circuit Cell Routing (Parasitic Aware)
Two Steps:
1. Critical Nets Routing Aware of Geometry and Proximity Constrains
2. Non-critical Nets routing
Means of In-situ Parasitic Extraction
245
Means of Circuit Performance Assurance
250
Means of Circuit Physical Layout Floor Planning
255

FIG. 2